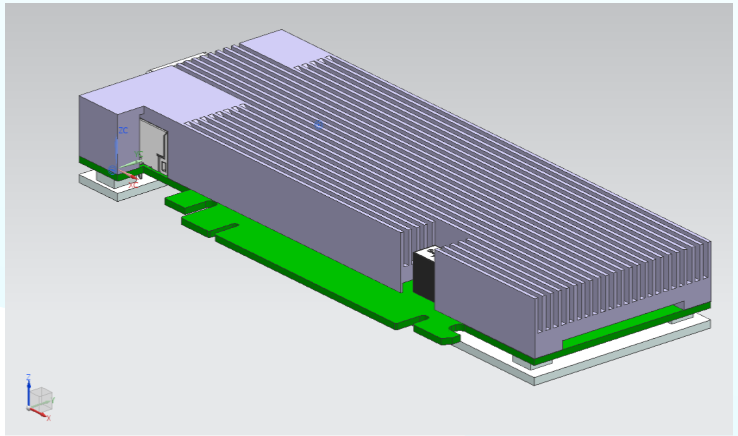
THERMAL MANAGEMENT OF PCIE CARD

Introduction

PCIe (Peripheral Component Interconnect Express) card:

- Thermal management is a critical aspect of PCIE cards to ensure optimal performance and longevity.
- This case study involves calculating thermal resistances throughout the system and selecting or designing appropriate heat sinks.
- In the case study, the objective is to determine the minimum mass flow rate required for dissipating heat generated by PCIe cards.
- To validate the design, we employ Computational Fluid Dynamics (CFD) simulations at various mass flow rates, providing insights into fluid flow patterns and heat dissipation capabilities.



PCIe card assembly (Trimetric View)

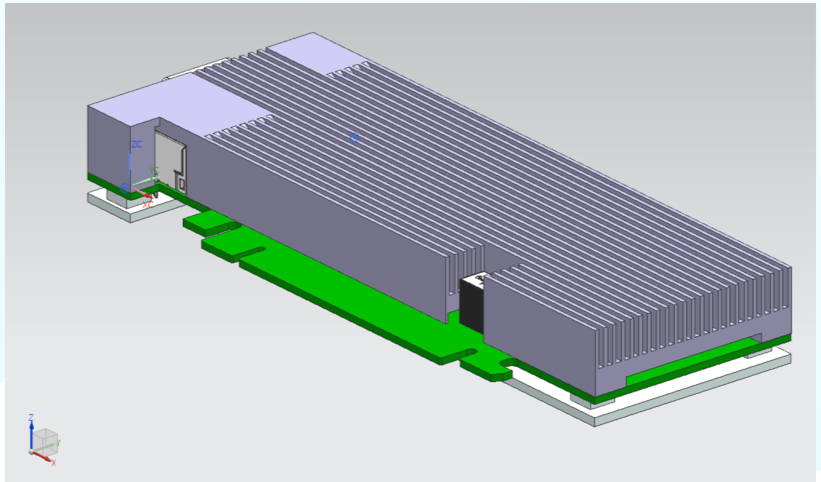
THERMAL MANAGEMENT OF PCIE CARD

Objective:

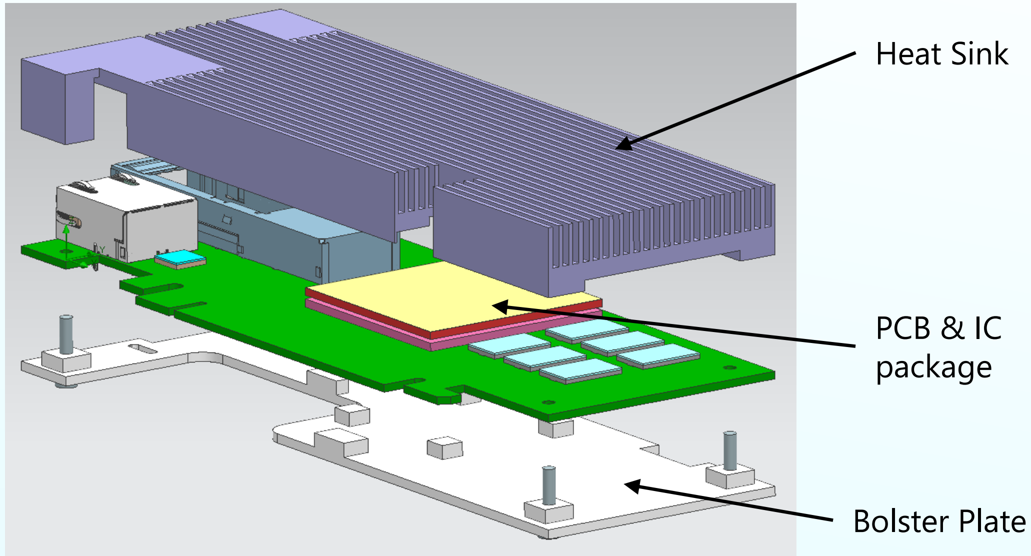
- Calculate thermal resistances across the system, design/choose suitable heat sink for effective dissipation of heat to achieve the junction temperature at die and other specification requirements.
- Perform thermal-CFD simulations and optimize the design iteratively to ensure the design intent is met.

Methodology:

- Perform first order calculations (analytical) for computation of heat transfer coefficient and minimum mass flow rate required to dissipate generated heat for given power loss and specifications requirement of the system.
- Perform CFD simulation at different mass flow rates to validate the design and ensure the specifications requirement are met.

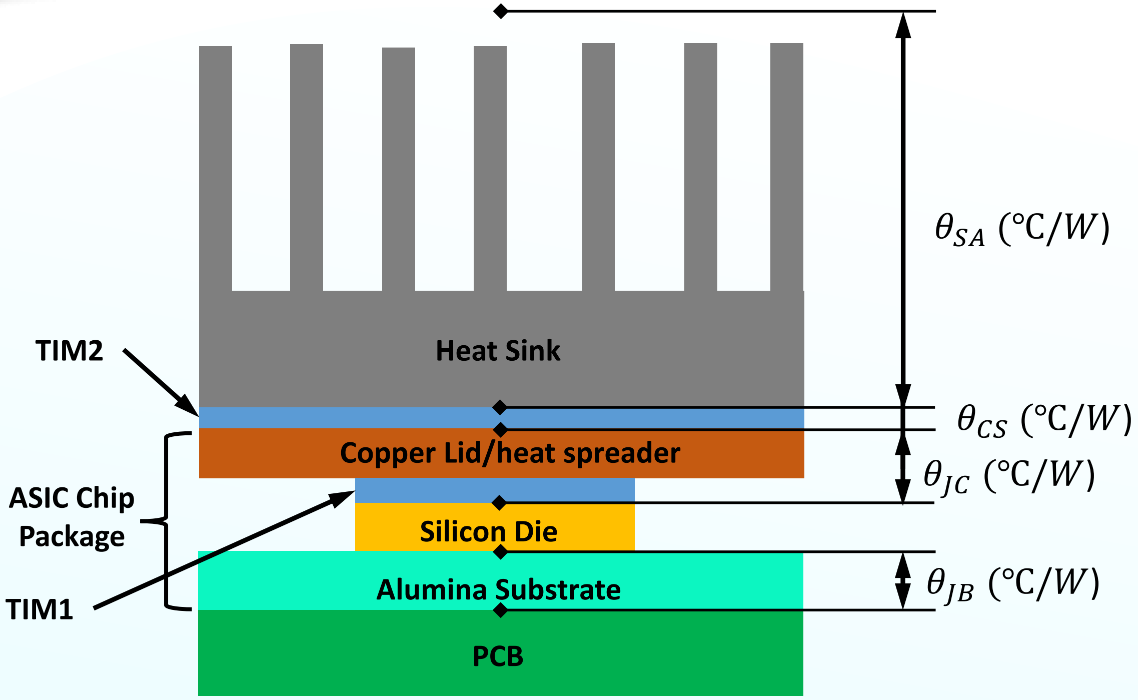


PCIe card assembly (Trimetric View)

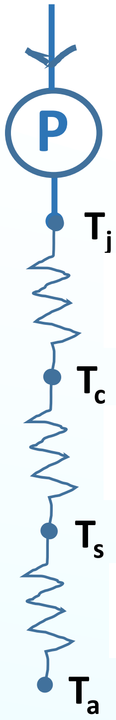


PCIe card assembly (exploded view)

THERMAL CIRCUIT ANALYSIS FOR PCIE CARD:



TYPICAL LIDDED PACKAGE



$$\theta_{JC} = \frac{T_j - T_c}{P}$$

$$\theta_{CS} = \frac{T_c - T_s}{P}$$

$$\theta_{SA} = \frac{T_s - T_a}{P}$$

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

$$\theta_{JA} = \frac{T_J - T_a}{P} = *** \ {}^0\mathrm{C/W}$$

$$\theta_{SA} = \theta_{JA} - (\theta_{JC} + \theta_{CS}) = *** \ {}^0\mathrm{C/W}$$

$$h_{conv} = \frac{1}{\eta_0 \times \theta_{SA} \times A_S} =*** \ \mathrm{W/m^2.{}^0C}$$

Where,

θ_{JA} - thermal resistance from Junction to Ambient
θ_{JC} - thermal resistance from Junction to Case
θ_{CS} - thermal resistance from Case to Sink
θ_{SA} - thermal resistance from Sink to Ambient
η_0 - overall fin efficiency
h_{conv}- *average convective heat transfer coefficient*
T_J - *Junction temperature*
T_c - *Case temperature*
T_s - *Sink temperature*
T_a - *Ambient temperature*

- Sink to Ambient thermal resistance is calculated from the thermal circuit analysis and average heat transfer coefficient is then computed.

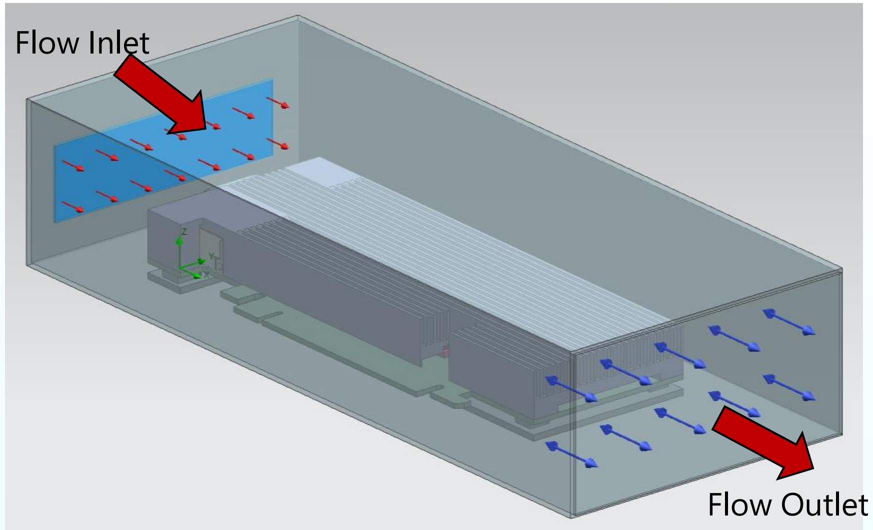
Parameter	Value	Unit	Remarks
Total power loss, P	***	W	
Required Junction temperature, Tj	***	deg C	
Ambient temperature, Ta	***	deg C	
Theta j-a	***	deg C/W	
Theta j-c	***	deg C/W	
Theta c-s	***	deg C/W	Thermal resistance across TIM
Theta s-a	***	deg C/W	
Surface area of heat sink, As	***	M2	
Overall fin efficiency, η_0	***	-	(Assumed value)
Required average convective heat transfer coefficient, h conv	YYY	W/m2-C	

Assumptions:

- **Overall/average heat transfer coefficient is calculated by disregarding radiative heat transfer for a junction temperature of *** ^{0}C.**
- **All surfaces of the heat sink are at isothermal condition.**

BOUNDARY CONDITIONS

Boundary Conditions:



PCIe card with flow domain

Altitude	Boundary	Boundary Condition	Volume flow rate (CFM)	Pressure (Pa)	Temperature (^{0}C)
Sea level	Inlet	Volume flow Inlet	3,9,15,30	101325	40
	Outlet	Static Pressure	-	101325	-
6000ft	Inlet	Volume flow Inlet	27,30,33 & 36	81196	40
	Outlet	Static Pressure	-	81196	-

Parametric Study(Sea Level conditions):

This following parameters were studied to meet the specification requirements.

- Heat sink material is changed from Al-6061 to Al-6063 to improve heat transfer rate.
- Different emissivity values were considered for Heat sink to improve radiative heat transfer coefficient.
  a. Aluminium polished surface (emissivity=0.07)
  b. Aluminium oxidized (emissivity=0.4) and
  c. Aluminium anodized (emissivity=0.8) were studied
- Multiple simulations were performed to study effect of volume flow rate on temperature.

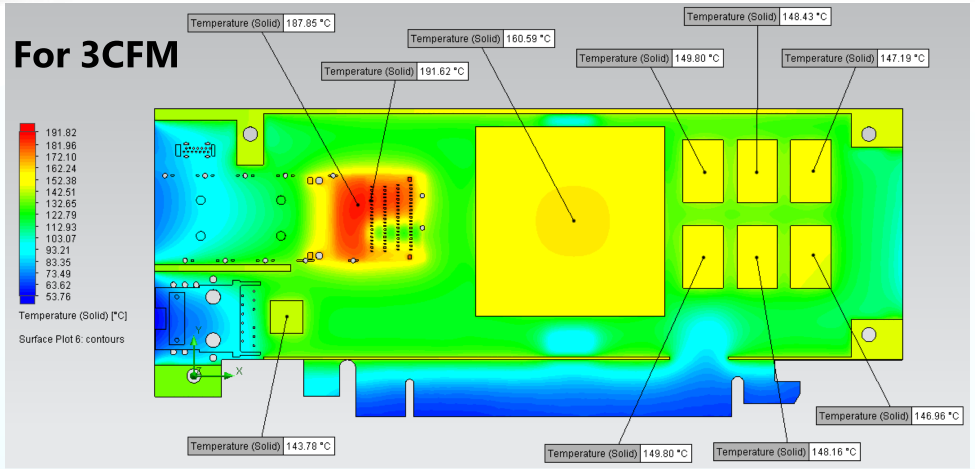
Component type	(3 CFM)* Max.Temperature. [^{0}C]	(3 CFM)** Temperature drop in %	(3 CFM)*** Temperature drop in %	(9CFM)* Temperature drop in %	(15 CFM)* Temperature drop in %	(30 CFM)* Temperature drop in %
ASIC Die	**xxx**	**5.0**	**1.2**	**18.0**	**27.5**	**41.4**
DDR	**xxx**	**5.5**	**0.3**	**19.0**	**28.9**	**44.3**
QSFP Connector	**xxx**	**2.7**	**0.1**	**14.8**	**24.9**	**38.2**
Ethernet Phy	**xxx**	**5.7**	**0.3**	**22.0**	**33.2**	**48.6**
Heat Sink	**xxx**	**5.2**	**0.7**	**18.8**	**28.5**	**42.6**
PCB	**xxx**	**2.6**	**0.2**	**16.9**	**27.8**	**41.5**
Solder Bump	**xxx**	**5.5**	**0.4**	**19.0**	**29.0**	**44.4**

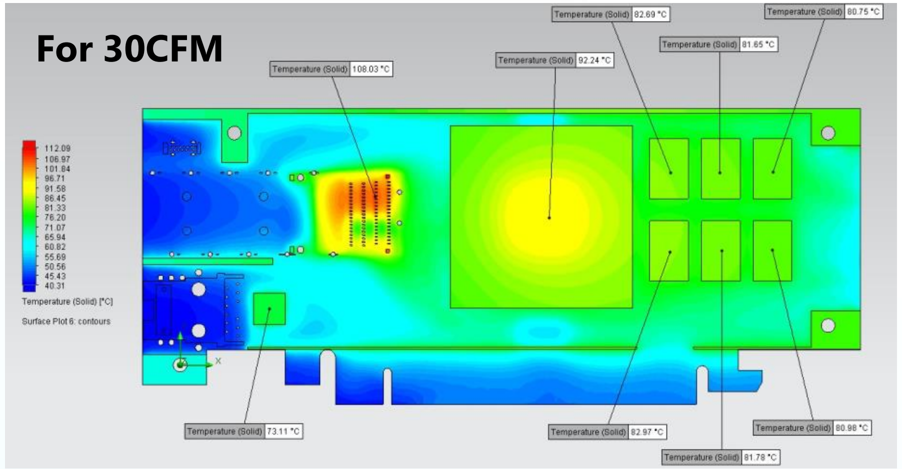
* Heat sink material as oxidized Al 6061 (emissivity 0.4)

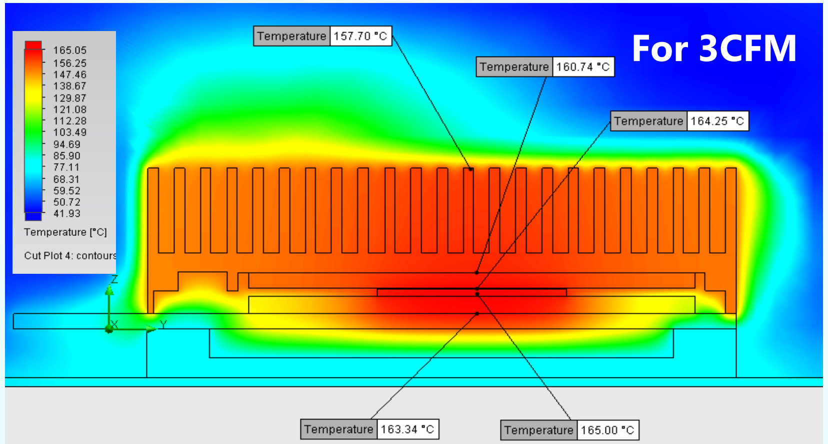
** Heat sink material as anodized Al 6061 (emissivity 0.8)

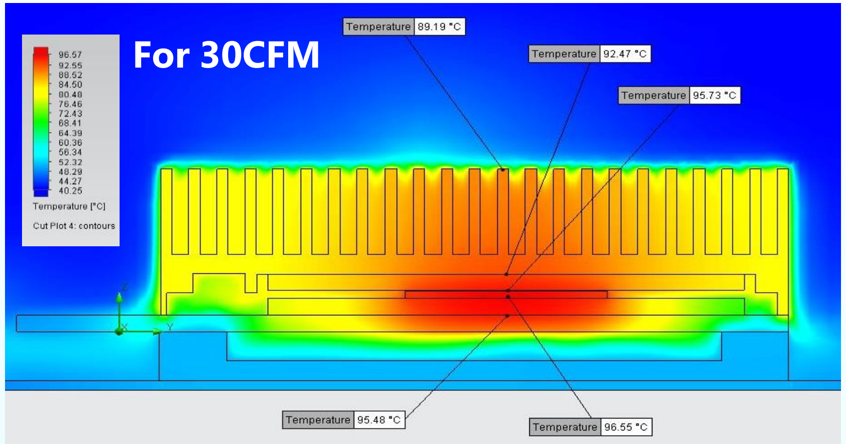
*** Heat sink material as oxidized Al 6063 (emissivity 0.4)

Temperature Plots-Comparison for varied flow rate:



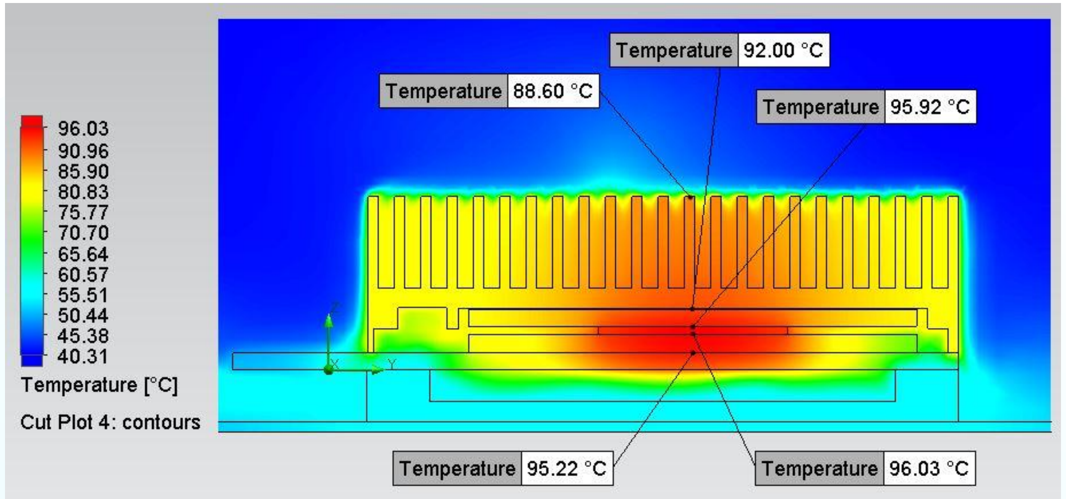




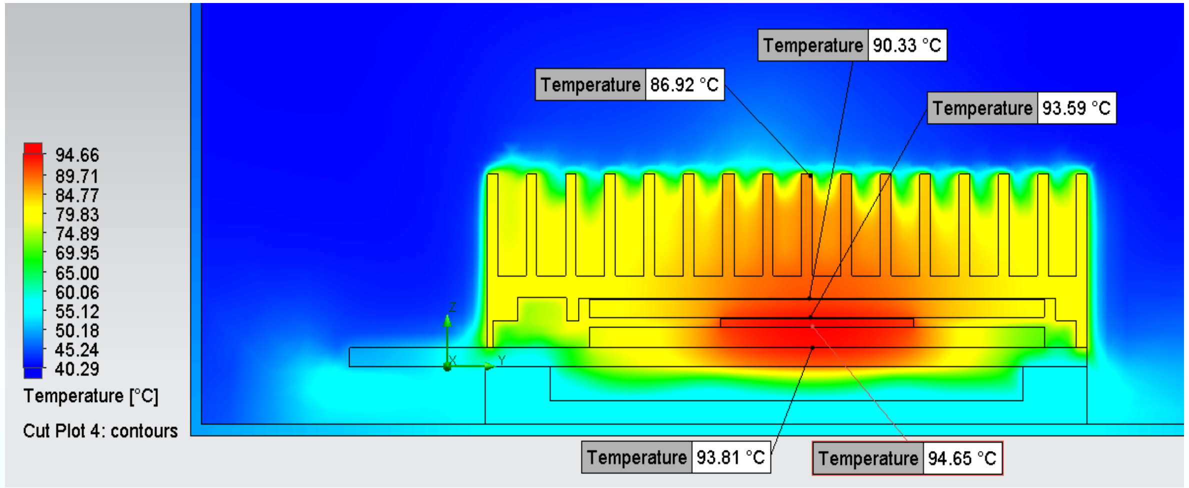


- When compared results of PCIe card for flow rate of 3CFM with 30CFM:
  - ASIC die temperature has dropped by about 71.4 ^{0}C (41.4%)
  - DDR temperature has dropped by about 70.0 ^{0}C (44.3%)
  - Ethernet Phy temperature has dropped by about 73.7 ^{0}C (48.6%)

Temperature Plots-Comparison for varied fin number:



Number of Fins : 23
Flow Rate : 27 CFM



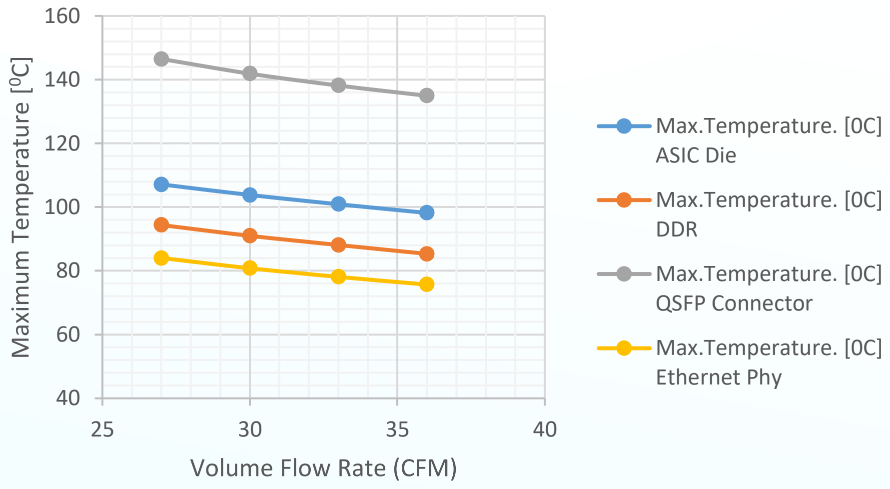
Number of Fins : 16
Flow Rate : 27 CFM

- When compared results of 16 fin heat sink model with 23 fin on the heat sink:
  - ASIC die temperature has dropped by about 1.3 ^{0}C (1.5%)
  - DDR temperature has dropped by about 2.9 ^{0}C (3.5%)
  - Ethernet Phy temperature has dropped by about 1.9 ^{0}C (2.6%)

Parametric Study(6000ft conditions):

Multiple simulations were performed to study effect of volume flow rate on temperature for 6000ft altitude conditions.

Component type	(3 CFM) Max.Temperature. [^{0}C]	(27 CFM) Temperature drop in %	(30 CFM) Temperature drop in %	(33 CFM) Temperature drop in %	(36 CFM) Temperature drop in %
ASIC Die	**xxx**	**37.4**	**39.4**	**41.1**	**42.6**
DDR	**xxx**	**44.9**	**46.8**	**48.5**	**50.2**
QSFP Connector	**xxx**	**14.4**	**17.1**	**19.3**	**21.1**
Ethernet Phy	**xxx**	**50.9**	**52.8**	**54.4**	**55.8**
Heat Sink	**xxx**	**40.0**	**41.9**	**43.6**	**45.2**
PCB	**xxx**	**27.0**	**29.3**	**31.3**	**33.0**
Solder Bump	**xxx**	**44.9**	**46.8**	**48.5**	**50.2**



Benefits:

- Performed CFD analysis on the initial design; Junction and case temperatures of the IC packages were found to be exceeding the limitations for the given flow rate as per specification requirements. Hence there was a need for higher air flow rates to meet the requirements which were evaluated through simulation.
- The evaluated flow rate allows to keep the temperatures with in limits and ensure reliable performance of the card for its extreme operating conditions.
- The modified design of the heat sink will bring down the temperatures further by about 4% there by increasing its performance.
- Customer saved both in prototyping and development cost.

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THANK YOU

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